What is claimed is:

1. A semiconductor test system, comprising:

a handler for moving and classifying semiconductor packages;

a logic tester for receiving a semiconductor package from the handler, and for testing a logic component of the semiconductor package;

an analog tester coupled to the logic tester, the analog tester for testing an analog component of the semiconductor package; and

an interface unit for selectively outputting a logic signal to enable the analog tester.

2. The system as claimed in claim 1, wherein the handler faces a sidewall of the logic tester, the handler further for controlling operation and stoppage of the logic tester and the analog tester.

3. The system as claimed in claim 1, further comprising a test board installed on a sidewall of the logic tester, between the handler and the logic tester, the test board being positioned on the sidewall of the logic tester in a vicinity of the semiconductor package received from the handler.

4. The system as claimed in claim 3, wherein the test board includes a logic terminal for connecting to the logic component of the semiconductor package and an analog terminal for connecting to the analog component of the semiconductor package.

5. The system as claimed in claim 4, wherein the analog tester is electrically coupled to the analog terminal of the test board.

6. The system as claimed in claim 3, further comprising a storage unit for storing test results of the logic tester.

7. The system as claimed in claim 6, wherein the storage unit is a latch circuit.

8. The system as claimed in claim 1, wherein the interface unit further includes a logic signal generating unit for selectively outputting a logic signal during the analog test.

9. The system as claimed in claim 8, wherein the logic signal generating unit is a multi-point control unit.

10. A semiconductor test system, comprising:

a handler for moving and classifying semiconductor packages;

a logic tester having a test board for receiving a semiconductor package from the handler, the test board mounted on a side wall of the logic tester facing the handler, the logic tester for testing a logic component of the semiconductor package mounted on the test board;

an analog tester coupled to the test board, the analog tester for testing an analog component of the semiconductor package that is decided as operationally functional during the logic test; and

an interface unit for selectively outputting a logic signal during the analog test.

11. The system as claimed in claim 10, wherein the handler outputs start of test signals and end of test signals to the logic tester and the analog tester.

12. The system as claimed in claim 10, wherein the test board includes a logic terminal for connecting to the logic component of the semiconductor package and an analog terminal for connecting to the analog component of the semiconductor package.

13. The system as claimed in claim 12, wherein the analog tester is electrically coupled to the analog terminal of the test board.

14. The system as claimed in claim 12, further comprising a storage unit for storing test results of the logic tester.

15. The system as claimed in claim 14, wherein the storage unit is a latch circuit

16. The system as claimed in claim 10, wherein the interface unit further includes a logic signal generating unit for selectively outputting a logic signal during the analog test.

17. A method of operating a semiconductor test system, comprising:

mounting a semiconductor package on a board of a logic tester;

testing a logic component of the semiconductor package with the logic tester; and

if the logic component of the semiconductor package is determined operationally functional, testing an analog component of the semiconductor package with an analog tester.

18. The method according to claim 17, further comprising classifying the semiconductor package as faulty if the logic component is determined operationally defective.

19. The method according to claim 17, further comprising classifying the semiconductor package as a operationally functional unit if both the logic and analog component tests determine the components are operationally functional.

20. The method as claimed in claim 17, wherein testing the analog component of the semiconductor package occurs while a logic signal is generated by a logic generating unit.

21. A semiconductor testing device, comprising:

a first testing unit for testing at least a section of a semiconductor device; and

an second testing unit for testing at least another section of the semiconductor device, the second testing unit testing the at least another

section of the semiconductor device if the first testing unit determines the at least a section is operationally functional.

22. The semiconductor testing device according to claim 21, wherein the first testing unit tests a logic section of the semiconductor device.

23. The semiconductor testing device according to claim 22, wherein the second testing unit is capable of testing an analog section of the semiconductor device.

24. The semiconductor testing device according to claim 21, further comprising an interface device for selectively enabling the second testing unit.

25. A method, comprising:

testing an analog component of a semiconductor device if it is determined a logic component of the semiconductor device is operationally functional.

26. The method according to claim 25, further comprising classifying the semiconductor device as defective if the logic component of the semiconductor device is not operationally functional.

27. The method according to claim 25, further comprising testing the logic component of the semiconductor device.

28. The method according to claim 23, further comprising producing a logic signal to enable testing the analog component of the semiconductor device.